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Improved electrical properties of n - n and p - n Si/SiC junctions with thermal annealing treatment

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The effects of annealing process on the electrical properties of n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions fabricated by using surface-activated bonding are investigated. It is found by measuring the current-voltage (I - V) characteristics of n^+ -Si/ n -SiC junctions that the reverse-bias current and the ideality factor decreased to 2.0×10^{-5} mA/cm² and 1.10, respectively, after the junctions annealing at 700 °C. The flat band voltages of n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions obtained from capacitance-voltage (C - V) measurements decreased with increasing annealing temperature. Furthermore, their flat band voltages are very close to each other irrespective of the annealing temperature change, which suggests that the Fermi level is still pinned at the bonding interface even for the junctions annealing at high temperature and the interface state density causing Fermi level pinning varies with the junctions annealing. The reverse characteristics of n^+ -Si/ n -SiC junctions are in good agreement with the calculations based on thermionic field emission. In addition, the calculated donor concentration of 4H-SiC epi-layers and flat band voltage is consistent with the values obtained from C - V measurements. *Published by AIP Publishing.*

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I. INTRODUCTION

Silicon carbide (SiC) is the best placed wide bandgap semiconductor for the next generation of power devices due to its advantageous material properties and the maturity of processing technology.^{1,2} Furthermore, it has been extensively studied for high-power electronics application. The combination of SiC with Si technologies could provide the promise for extending electronic applications in areas requiring high-frequency operation, high power, and high temperature environments. Si/SiC heterojunction is a potentially useful system for realizing high-performance bipolar transistors with wide band gap emitters,^{3,4} switching devices,⁵ electroluminescence devices,⁶ and sensors.⁷ On the other hand, it is difficult to directly grow the SiC layers on the Si substrates without buffer layers due to the large lattice mismatch and the difference in thermal expansion coefficients between Si and SiC. The formation of Si/SiC heterojunction using conventional crystal growth method is likely to have high defects and dislocation densities. Although there are a few reports on the fabrication of Si/SiC heterojunctions,^{8,9} the growth of SiC layers on the Si substrates results in junctions with low breakdown voltage and high reverse-bias current possibly due to the low-temperature growth of SiC films.

Heterojunctions of materials with difference in crystal structures, lattice constants, and thermal expansion coefficients have been realized by using surface activated bonding (SAB), in which the sample surfaces are activated by Ar fast atom beams in a high vacuum prior to bonding in low temperatures.^{10,11} We previously fabricated and characterized Si/SiC heterojunctions.^{12,13} The reverse leakage currents of

p -Si/ n -4H-SiC junctions were decreased and their ideality factors were improved by annealing them at higher temperatures. Furthermore, the conduction band offset and the density of interface states were estimated by analyzing the capacitance-voltage characteristics of n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions. In addition, we have applied Si/4H-SiC heterojunctions into heterojunction bipolar transistors and investigated their electrical characteristics.¹⁴ Despite the common-base characteristics were obtained, the current gain was very small at room temperature. Since the low current gain should be attributed, the large number of interface states is formed at the bonding interface. It is assumed that the interface states with high density are formed at the bonding interface due to the irradiation of Ar atom beams. Our previous results showed that the interface state density in SAB-based Si/Si junctions could be improved by annealing the junctions at high temperature in N₂ gas ambient.¹⁵ Although the reverse-bias current of p^+ -Si/ n -SiC junctions is greatly reduced by annealing the junctions at high temperature and the interface state density of Si/SiC junctions without annealing was obtained, the behavior of the interface state density with annealing temperature on the electrical properties of n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions is still unclear. It is very important to control the carrier transport across the interface of Si/SiC heterojunctions.

In this work, we systematically studied the effects of thermal annealing process on the electrical properties of n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions. Their electrical properties were investigated by measuring current-voltage (I - V) and capacitance-voltage (C - V) characteristics. Furthermore, we discussed the correlation among the electrical properties of the interface, the interface state density, and the annealing temperature.

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II. EXPERIMENTS

A. Method

B-doped (100) p^+ -Si substrates, P-doped (100) n^+ -Si substrates, and n-4H-SiC epitaxial substrates ($6\ \mu\text{m}$, $\sim 5 \times 10^{15}\ \text{cm}^{-3}$ epitaxial layer/ $0.5\ \mu\text{m}$, $>1 \times 10^{18}\ \text{cm}^{-3}$ buffer layer/substrate $\sim 3 \times 10^{18}\ \text{cm}^{-3}$) were used for the bonding experiment. The Hall measurements at room temperature revealed that the resistivities and carrier concentrations were $0.003\ \Omega\cdot\text{cm}$ and $(N_{A=})\ 2.64 \times 10^{19}\ \text{cm}^{-3}$, and $0.002\ \Omega\cdot\text{cm}$ and $(N_{D=})\ 2.64 \times 10^{19}\ \text{cm}^{-3}$ for the p^+ -Si and n^+ -Si substrates, respectively. Before bonding, Al/Ni/Au multilayers were evaporated on the back surfaces of the n-SiC substrates. The Ohmic contacts of n-SiC substrates were formed by rapid thermal annealing at $1000\ ^\circ\text{C}$ for 1 min in N_2 gas ambient. The n-4H-SiC epitaxial substrates and two types of Si substrates were bonded to each other by SAB,^{16–18} so that n^+ -Si/n-SiC and p^+ -Si/n-SiC junctions were fabricated. And then, the bonded samples were annealed separately at 400 and $700\ ^\circ\text{C}$ for 1 min in the N_2 gas ambient. After the bonding, the Al/Ni/Au and Ti/Au multilayers were evaporated on the back side surfaces of the p^+ -Si and n^+ -Si substrates, respectively, and the Ohmic contacts of p^+ -Si substrates were achieved by rapid thermal annealing at $400\ ^\circ\text{C}$ for 1 min in N_2 gas ambient. The other p^+ -Si/n-SiC and n^+ -Si/n-SiC junctions were fabricated by forming Ohmic contacts on each of the n-SiC, p^+ -Si, and n^+ -Si substrates and bonding them. The characteristics of these two samples were investigated, while the junctions were unannealed. All of the bonded samples were diced into $4\ \text{mm}^2$ pieces. Their I - V and C - V characteristics were measured using an ADCMT 6242 Source Measurement Unit and an Agilent E4980A Precision Impedance Analyzer, respectively.

B. Results

The I - V characteristics of n^+ -Si/n-SiC junctions measured at room temperature are shown in Fig. 1. A hump was observed in the I - V characteristics of the unannealed junction at low forward-bias voltages. The hump becomes less pronounced after annealing at 400 and $700\ ^\circ\text{C}$. The ideality

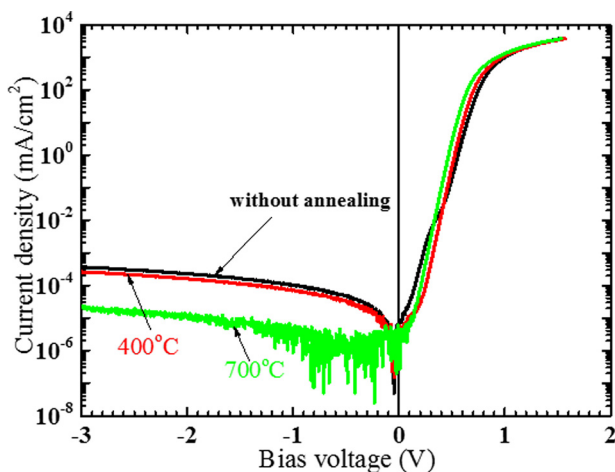


FIG. 1. I - V characteristics of n^+ -Si/n-SiC junctions without being annealed and annealed at 400 and $700\ ^\circ\text{C}$ measured at room temperature.

factor between 0.3 and 0.5 V was extracted to be 1.64, 1.15, and 1.10 for the unannealed junction and the junctions annealed at 400 and $700\ ^\circ\text{C}$, respectively. The magnitude of the current increased as the junctions were more deeply reverse biased. Furthermore, the magnitude of the current at $-3\ \text{V}$ decreased significantly from 3.71×10^{-4} to $2.0 \times 10^{-5}\ \text{mA/cm}^2$ as the annealing temperature increased up to $700\ ^\circ\text{C}$. In addition, the noise curve was observed between 0 and $-1.8\ \text{V}$ for the junction annealed at $700\ ^\circ\text{C}$, which is due to the resolution limit of the measurement unit. The series resistance of the respective junctions was extracted from the slope of the I - V characteristics between 0.8 and 1.5 V. It is found that the resistance remained constant as the annealing temperature increased. Moreover, it can be seen that the turn-on voltage of the junctions, which was defined as the forward-bias voltage for the current of $100\ \text{mA/cm}^2$, decreased from 0.75 to 0.65 V as the annealing temperature increased. Their parameter values for the respective junctions are summarized in Table I.

The C - V characteristics of n^+ -Si/n-SiC and p^+ -Si/n-SiC junctions were performed at a room temperature and a frequency of 100 kHz. The results for n^+ -Si/n-SiC and p^+ -Si/n-SiC junctions are shown in Figs. 2(a) and 2(b), respectively. The characteristics indicated a straight line and their flat band voltages (V_d) were found to be 0.91, 0.9, and 0.85 V and 0.92, 0.89, and 0.88 V for n^+ -Si/n-SiC and p^+ -Si/n-SiC junctions without being annealed and annealed at 400 and $700\ ^\circ\text{C}$, respectively, by linearly extrapolating $1/C^2$ to zero. It is noteworthy that the flat band voltages of n^+ -Si/n-SiC and p^+ -Si/n-SiC junctions concurrently decrease with the annealing temperature increasing; furthermore, their flat band voltages are highly close to each other, irrespective of the polarity of Si substrates and the annealing temperature of the junctions. In addition, the $1/C^2$ - V characteristics of n^+ -Si/n-SiC and p^+ -Si/n-SiC junctions were also measured at room temperature and frequencies between 1 kHz and 1 MHz. However, the frequency dispersions were not observed on the bias voltage between -3 and 0 V (not shown in this figure). Using the slopes of $1/C^2$ - V characteristics, the donor concentrations (N_d) of the n-SiC epitaxial layers were estimated to be 3.12×10^{15} , 3.20×10^{15} , and $3.13 \times 10^{15}\ \text{cm}^{-3}$; and 3.10×10^{15} , 3.22×10^{15} , and $3.24 \times 10^{15}\ \text{cm}^{-3}$ for n^+ -Si/n-SiC and p^+ -Si/n-SiC junctions without being annealed and annealed at 400 and $700\ ^\circ\text{C}$, respectively. The obtained donor concentrations are small compared with our previous reports for Ni/n-SiC Schottky diodes.¹³ Their values obtained from the slope and intersection of $1/C^2$ - V plots are summarized in Table II.

TABLE I. The reverse-bias current, turn-on voltage, ideality factor, and resistance of n^+ -Si/n-SiC heterojunctions.

Annealing temperature	Reverse-bias current (mA/cm^2)	Turn-on voltage (V)	Ideality factor	Resistance ($\Omega\cdot\text{cm}^2$)
Without annealing	3.71×10^{-4}	0.75	1.64	0.20
400 $^\circ\text{C}$	2.65×10^{-4}	0.71	1.15	0.21
700 $^\circ\text{C}$	2.0×10^{-5}	0.65	1.10	0.22

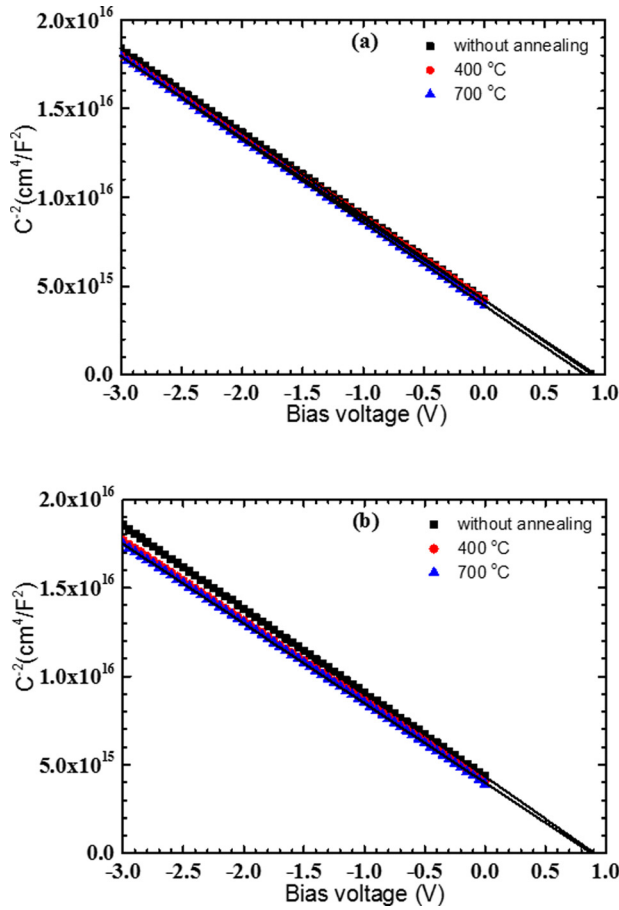


FIG. 2. C - V characteristics of (a) n^+ - Si/n - SiC and (b) p^+ - Si/n - SiC junctions without being annealed and annealed at 400 and 700 °C measured at room temperature.

Figures 3(a)–3(c) show the I - V characteristics of n^+ - Si/n - SiC junctions without being annealed and annealed at 400 and 700 °C, respectively, measured at various temperatures. The respective curves revealed a more marked asymmetric properties at low temperature. Note that the magnitude of the current increased with increasing depth of the reverse bias in each junction. The current also increased as the ambient temperature increased. The current of the reverse bias voltages after annealing at 700 °C is increased by $\sim 10^4$ times as the temperature increased up to 473 K. The slope of the current obtained at 358, 408, and 473 K between -3 and -1 V is not almost sensitive to the temperature of measurement. In comparison, the slope of the current decreased when the temperature of measurement was raised for the unannealed junction and the junction annealed at 400 °C.

TABLE II. Obtained parameters of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions by C - V measurements.

Annealing temperature	n^+ - Si/n - SiC junction		p^+ - Si/n - SiC junction	
	N_d (cm^{-3})	V_d (V)	N_d (cm^{-3})	V_d (V)
Without annealing	3.12×10^{15}	0.91	3.10×10^{15}	0.92
400 °C	3.20×10^{15}	0.9	3.22×10^{15}	0.89
700 °C	3.13×10^{15}	0.85	3.24×10^{15}	0.88

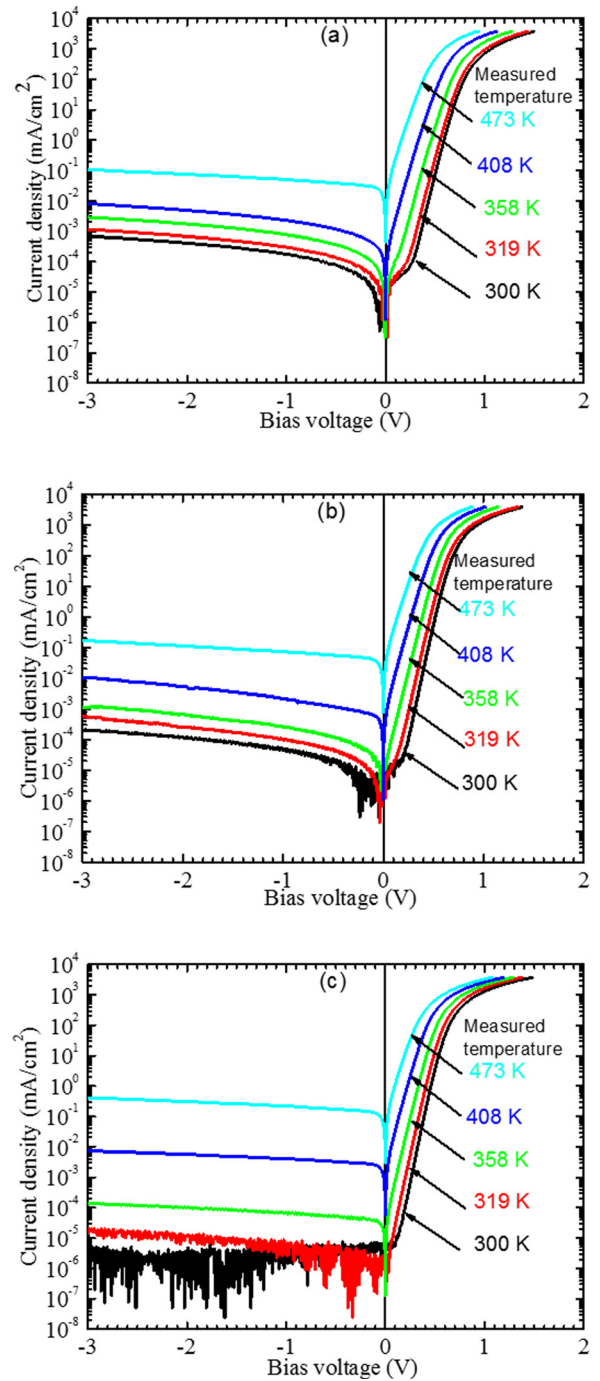


FIG. 3. Temperature dependence of the I - V characteristics of n^+ - Si/n - SiC junctions (a) without being annealed (Reprinted with permission from Appl. Phys. Lett. **105**, 151607 (2014). Copyright 2014 AIP Publishing LLC) and annealed at (b) 400 and (c) 700 °C measured at various temperatures.

The I - V characteristics of p^+ - Si/n - SiC junctions without being annealed and annealed at 400 and 700 °C measured at various temperatures are shown in Figs. 4(a)–4(c), respectively. The I - V characteristics of all the junctions showed good rectification properties at low temperatures. The magnitude of the reverse-bias current at -3 V decreased significantly as the annealing temperature increased. A noise curve of the reverse-bias current obtained at 300 K after annealing at 700 °C is also observed. The magnitude of the current increased with increasing the reverse-bias voltage and the

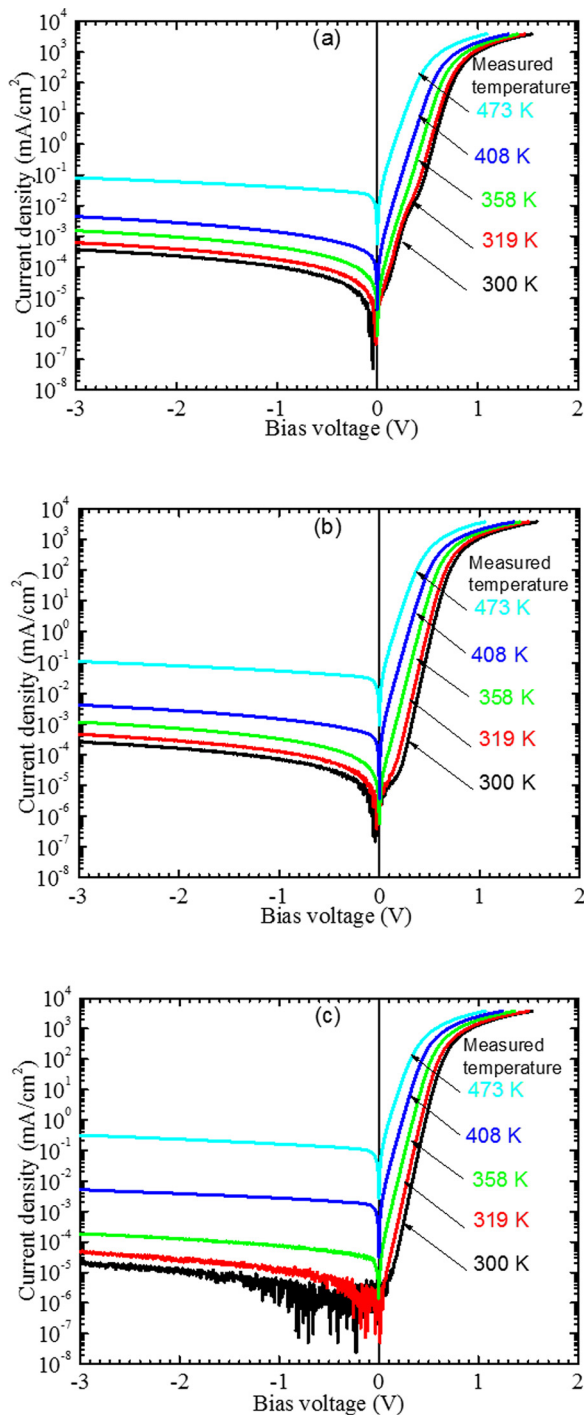


FIG. 4. Temperature dependence of the I - V characteristics of p^+ - Si/n - SiC junctions (a) without being annealed (Reprinted with permission from Appl. Phys. Lett. **104**, 161604 (2014). Copyright 2014 AIP Publishing LLC) and annealed at (b) 400 and (c) 700 °C measured at various temperatures.

measurement temperature in the unannealed junction and the junction annealed at 400 °C. It is notable that the slope of the current obtained at 358, 408, and 473 K after annealing at 700 °C between -3 and -1 V is almost invariant to the temperature. In comparison, the slope of the current for the unannealed junction and the junction annealed at 400 °C decreased as the measurement temperature increased.

The reverse I - V characteristics of n^+ - Si/n - SiC junctions without being annealed and annealed at 400 and 700 °C and

p^+ - Si/n - SiC junctions without being annealed and annealed at 700 °C are shown in Figs. 5(a) and 5(b), respectively. As expected, the magnitude of the reverse current increased with increasing reverse-biased voltage and the current density reached to 1.0×10^{-1} and 1.7×10^{-1} mA/cm² at -200 V for n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions without being annealed, respectively. Furthermore, the current density at -200 V decreased with increasing the annealing temperature. Finally, it decreased to 2.3×10^{-2} and 1.1×10^{-2} mA/cm² after annealing at 700 °C for n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions, respectively. Although the breakdown characteristics were not observed at -200 V for the respective junctions, a breakdown voltage more than 200 V should be expected in both n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions.

In the I - V characteristics of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions, the magnitude of the reverse-bias current depends on the bias voltage and the measurement temperature, which is similar to the wafer-fused p - $GaAs/n$ - GaN heterojunctions.¹⁹ The current at -3 V as a function of the measurement temperature is shown in Fig. 6. The data obtained at 27 °C for the p^+ - Si/n - SiC junction annealed at 700 °C are not shown in this figure because it is below the resolution of the measurement unit. We found that the reverse-bias current dependence on the temperature was approximately expressed

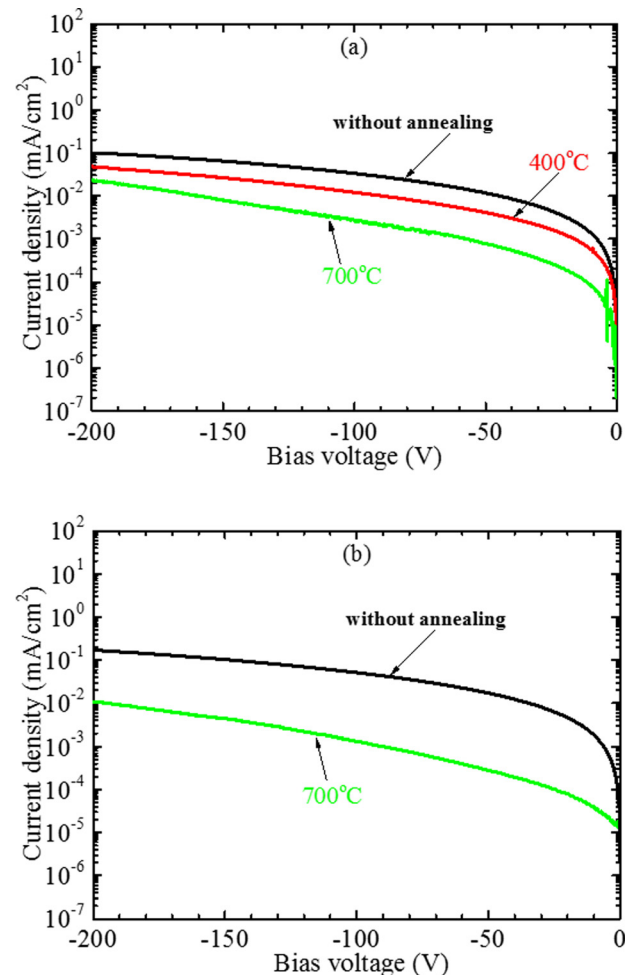


FIG. 5. Reverse I - V characteristics of (a) n^+ - Si/n - SiC junctions without being annealed and annealed at 400 and 700 °C and (b) p^+ - Si/n - SiC heterojunctions without being annealed and annealed at 700 °C.

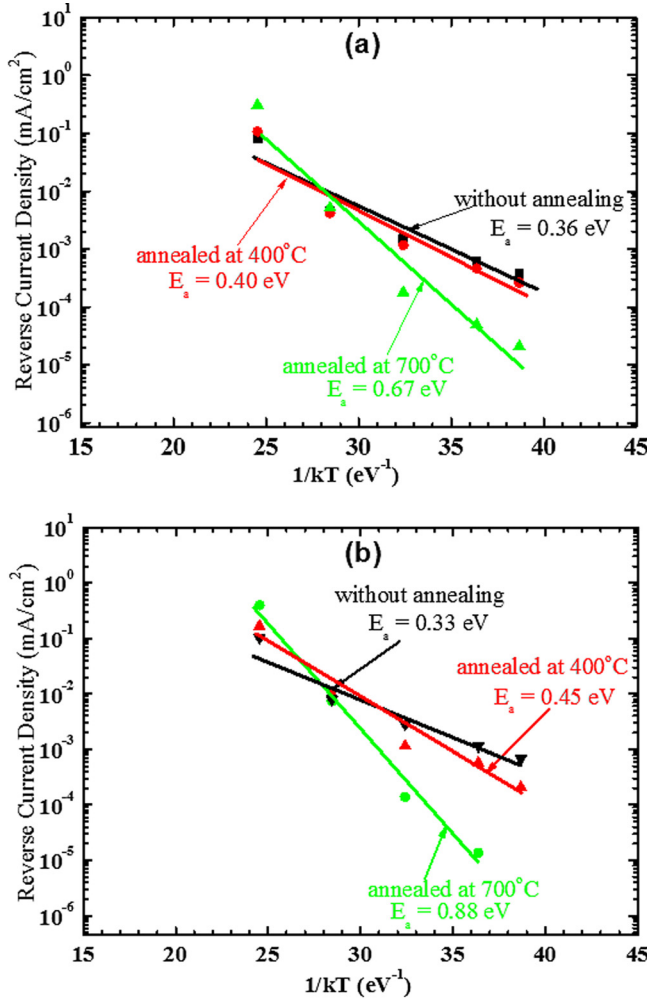


FIG. 6. Relationship of the reverse-bis current measured at -3 V for (a) n^+ - Si/n - SiC and (b) p^+ - Si/n - SiC junctions without being annealed and annealed at 400 and 700 °C.

as $I \propto \exp(-E_a/kT)$, where E_a is the activation energy. The value of the activation energy of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions was estimated to be 0.33, 0.40, and 0.67 eV and 0.33, 0.45, and 0.88 eV for the unannealed junction and junction annealed at 400 and 700 °C, respectively. In addition, it is found that the value of the activation energy increases as the annealing temperature increases for both n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions.

III. DISCUSSION

We found that the flat band voltage of n^+ - Si/n - SiC junctions decreased to 0.85 V after annealing at 700 °C, which is consistent with the turn-on voltage extracted from the I - V characteristics. Furthermore, this value almost equals to that of the n^+ - Si/n - SiC junctions with annealing at 700 °C. There is a large discrepancy between the flat band voltages of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions. For the p^+ - Si/n - SiC junctions, a much large flat band voltage should be expected since the difference between the flat band voltages of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions is close to silicon bandgap energy (1.12 eV).¹³ However, the obtained flat band voltages of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions are pretty close to

each other at each annealing temperature. This result should be attributed to the Fermi level pinning, which is due to the irradiation of Ar atom beams in the SAB process causing the high interface state density formed at the bonded interface. However, it should be recovered after the junctions annealing at high temperature. The interface state density dependence on the annealing temperature has been reported in the Si/Si and Si/GaAs junctions fabricated by SAB.^{15,20} It has been found that the interface state density at the Si/Si interface decreased with increasing the annealing temperature.

Note that if a large number of interface states still exist at the bonded interface, the large reverse-bias current should be observed. However, in the I - V characteristics of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions with annealing at 700 °C, the magnitude of the reverse-bias current is as low as 2.0×10^{-5} mA/cm², which is lower than the resolution of the measurement unit and is much smaller than those previously reported for n - Si/n - SiC ²¹ and p - Si/n - SiC ²² junctions fabricated by molecular beam epitaxy and direct wafer bonding, respectively. This results in disagreement with the above-mentioned results. It has been reported that the decrease in the interface state density brought about the lowering of the potential barrier height and significantly improved the conductive properties of the Si/Si junctions.¹⁵ Similar phenomenon is also observed in our n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions. Thus, we suggest that the flat band voltage decreases as the annealing temperature increases, which is due to the reduction of the interface state density. This result is in good agreement with the features the lowering of the reverse bias current and the improving of the ideality factor of the n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions with annealing. Furthermore, the estimated activation energy values of n^+ - Si/n - SiC and p^+ - Si/n - SiC junctions after annealing at 700 °C are also consistent with the flat band voltages obtained from the C - V characteristics. Consequently, we believe that although the thermal annealing process could not significantly decrease the interface state density, it could markedly improve the electrical properties of the bonded interfaces.

The features of the n - Si/n - SiC junctions in the I - V characteristics such as (1) increase in the current due to deeper reverse bias and (2) slope in the current variant to the measurement temperatures are similar to those for InS/Au ²³ and Si/Ni ²⁴ Schottky diodes. Moreover, we found that those features were consistent with the scheme of Thermionic Field Emission (TFE)²⁵ in comparison with the analyses by using other schemes for the carrier transport in reverse-biased junctions such as generation-recombination model,²⁶ Trap-assisted tunneling,²⁷ and Field Emission model.²⁸ Here, we used the simplified formula of TFE model²⁹ for the analysis of n^+ - Si/n - SiC junctions in the I - V characteristics

$$J_{TFE} = \frac{A^* T q \hbar E}{k} \sqrt{\frac{\pi}{2m_n k T}} \exp \left[-\frac{1}{kT} \left(\phi_B - \frac{(q \hbar E)^2}{24m_n (kT)^2} \right) \right], \quad (1)$$

where J_{TFE} is the observed current density of n^+ - Si/n - SiC junctions under forward bias voltage, m_n ($m_n = 0.29m_0$, m_0 is the electron rest mass)³⁰ is the electron effective mass, and

k , \hbar , and q are the Boltzmann constant, the Reduced Planck constant, and the electron charge, respectively. ϕ_B is the barrier height of the electron injections from the Si conduction band to the 4H-SiC conduction band. A^* is the effective Richardson constant which is calculated to be $36 \text{ A/cm}^2 \text{ K}^2$ by using the formula $A^* = \frac{4\pi m_n k^2}{h^3}$, where h is the Planck's constant. E is the electric field at the Si/SiC interface, which is given by

$$E = \sqrt{\frac{2qN_d(V_d - V)}{\epsilon_s \epsilon_0}}, \quad (2)$$

where V is the applied voltage, and ϵ_0 and ϵ_s are the permittivity of vacuum and the dielectric constant of 4H-SiC, respectively. For the relative dielectric constant (ϵ_s), a well-established reported value of 9.66 was used. Figure 7 shows the reverse I - V characteristics of n^+ -Si/ n -SiC junctions annealed at 700°C measured at various temperatures. The fitting curves using the TFE model are also shown in Fig. 7. A good fit was obtained for the respective curves, which suggests that the current due to the thermionic field emission was dominant at the reverse bias current. According to the fitting J versus V curve of the junctions, the donor concentration, flat band voltage, and barrier height were extracted to be $3.4 \times 10^{15} \text{ cm}^{-3}$, 0.72 V , and 0.81 eV , respectively. These values coincide with the values extracted from C - V characteristics. In addition, these results indicate that the TFE model can quantitatively explain the reverse bias currents of n^+ -Si/ n -SiC junctions, in which electrons in the conduction band edge of n^+ -Si were thermally excited at an energy level below the top of the barrier height of n^+ -Si contacts to n -SiC, then the electrons tunnel into the conduction band of the n -SiC. Furthermore, the barrier height obtained from the fitting of TFE model is close to the activation energy value of n^+ -Si/ n -SiC junctions. For the carrier across the interface of p^+ -Si/ n -SiC junctions, we have already explained in our previous report. The results of the present work suggest that the effects of the interface states on the carrier transport properties across the interface are likely to be removed by optimizing the condition of SAB process and changing annealing gas atmosphere such as hydrogen gas.

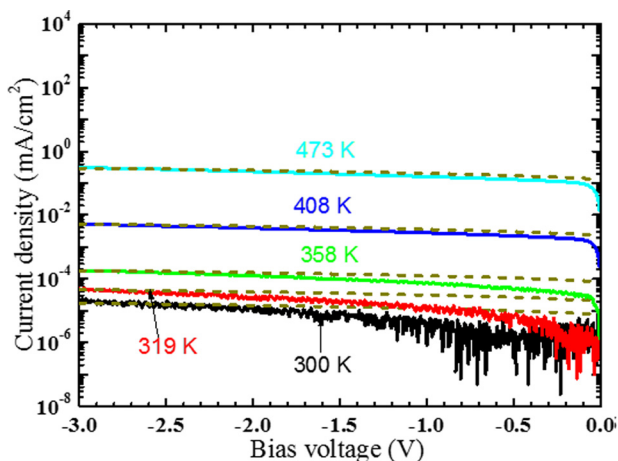


FIG. 7. Reverse I - V characteristics of n^+ -Si/ n -SiC junctions annealed at 700°C measured at various temperatures. The fitting curves using the thermionic-field emission theory are shown by a dotted line.

IV. CONCLUSION

We fabricated n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions by using surface activated bonding and demonstrated the influence of thermal annealing process on their electrical properties. For n^+ -Si/ n -SiC junctions with annealing at 700°C , the reverse-bias current at -3 V and the ideality factor were reduced to $2.0 \times 10^{-5} \text{ mA/cm}^2$ and 1.10, respectively. The flat band voltages of n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions decreased as the annealing temperature increased. Moreover, their flat band voltages are similar to each other even after the junctions annealing at high temperature. These results are attributed to Fermi-level pinning at their bonding interfaces and the interface state density varies with annealing temperature. The reverse I - V characteristics of n^+ -Si/ n -SiC junctions are in agreement with a theoretical calculation based on the TFE model with the donor concentration of $3.4 \times 10^{15} \text{ cm}^{-3}$ and the flat band voltage of 0.72 V . The reverse bias currents of n^+ -Si/ n -SiC and p^+ -Si/ n -SiC junctions may be further improved by optimizing the condition of SAB process, post-banding annealing temperature, and gas atmosphere. We believe that these experiments will provide much insight into the application of Si/SiC junctions for high-power devices.

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