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Effects of thermal annealing process on the electrical properties of p⁺-Si/n-SiC heterojunctions

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The effects of thermal annealing process on the interface in p⁺-Si/n-SiC heterojunctions fabricated by using surface-activated bonding are investigated. It is found by measuring their current-voltage (*I-V*) characteristics that the reverse-bias current and the ideality factor decreased to 2.98×10^{-6} mA/cm² and 1.03, respectively, by annealing the junctions at 1000 °C. Observation by using transmission electron microscopy indicates that an amorphous layer with a thickness of ~6 nm is formed at the unannealed interface, which vanishes after annealing at 1000 °C. No structural defects at the interface are observed even after annealing at such a high temperature. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4873113>]

Silicon carbide (SiC) has been extensively studied for high-power electronics application because of its unique physical properties, such as a wide band gap, high thermal conductivity, high electron saturation velocity, high physical, chemical stability, and high breakdown field.¹ The combination of SiC with Si technologies hold the promise for opening up electronic applications in areas requiring high-frequency operation, high power, and high temperature environments. Growth of SiC on Si to form heterojunctions is of considerable interest in realizing wide band gap emitters or window regions in bipolar transistors,² photo-detectors, and electroluminescence devices.³ However, the large lattice mismatch between Si and SiC has limited their intrinsic performance.⁴ It is found that growth of SiC layers on Si substrates results in junctions with low breakdown voltage, and high reverse-bias current,⁵⁻⁷ possibly due to the low-temperature growth of SiC films. One way to overcome these difficulties is direct wafer bonding which can accommodate the lattice mismatch between the bonding substrates. In the process of direct wafer bonding, however, thermal annealing at high temperatures is required so as to achieve enough bonding strength. There are a few literatures which have reported for direct wafer bonding-based Si/SiC heterojunctions⁸⁻¹¹ and Si/6H-SiC-based MOSFETs devices.¹² The influences of annealing process on the electrical and structural behaviors of the Si/SiC heterojunctions have not yet been reported. An alternative approach to achieve Si/SiC heterojunctions with high mechanical strength can be realized by using surface-activated bonding (SAB). SAB, in which surfaces of substrates are activated by the fast atom beams of Ar prior to bonding, has enabled us to bond substrates without annealing.¹³⁻¹⁷

In this work, we studied the effects of thermal annealing process on the electrical properties of p⁺-Si/n-SiC heterojunction. The electrical properties of the p⁺-Si/n-SiC junctions without annealing and after annealing were investigated by measuring their current-voltage (*I-V*) characteristics. The structural properties of the interfaces were examined by transmission electron microscopy (TEM) observation. The

applicability of Si/SiC heterojunctions for functional devices was explored based on these measurements.

B-doped (100) p⁺-Si substrate and n-4H-SiC epitaxial substrates (6 μm, ~5 × 10¹⁵ cm⁻³ epitaxial layer/0.5 μm, >1 × 10¹⁸ cm⁻³ buffer layer/substrate ~3 × 10¹⁸ cm⁻³) were used for the bonding experiment. The Hall measurements at room temperature revealed that the resistivity and carrier concentration were 0.003 Ω·cm and 2.6 × 10¹⁹ cm⁻³ for the p⁺-Si substrates, respectively. Before bonding, Al/Ni/Au multilayers were evaporated on the backside of three n-SiC substrates. The ohmic contacts of n-SiC substrates were formed by a rapid thermal annealing at 1000 °C for 60 s in N₂ gas ambient. These substrates and three p⁺-Si substrates were bonded to each other by using SAB.¹⁵⁻¹⁷ And then, the bonded samples were annealed separately at 400, 700, and 1000 °C for 60 s in N₂ gas ambient. After the bonding, Al/Ni/Au multilayers were evaporated on the backside of p⁺-Si substrates, and ohmic contacts were achieved by annealing them at 400 °C for 60 s. Another bonding sample was fabricated by forming ohmic contacts on each of n-SiC and p⁺-Si substrates and bonding them. The characteristics of this sample were investigated while the junction was unannealed. All of the four bonded samples were diced into 4 mm² pieces. We measured their *I-V* characteristics using an Agilent B2902A Precision Measurement Unit. The bonding interfaces of the p⁺-Si/n-SiC junctions were investigated using TEM (JEOL JEM-2100).

The *I-V* characteristics measured at room temperature are shown in Fig. 1. A hump is observed in the *I-V* characteristics of the unannealed junction at low forward-bias voltages. The hump becomes much smaller after annealing at 400 °C. It disappeared when the junctions were annealed at temperatures above 700 °C. The ideality factor for the forward bias voltages between 0.2 and 0.5 V was extracted to be 1.32, 1.15, 1.1, and 1.0 for the unannealed junction and junctions annealed at 400, 700, and 1000 °C, respectively. The magnitude of the current increased as the junctions were more deeply reverse biased. Furthermore, as the annealing temperature increased, the magnitude of the reverse-bias current at -3 V decreased significantly from 7.20 × 10⁻⁴ to

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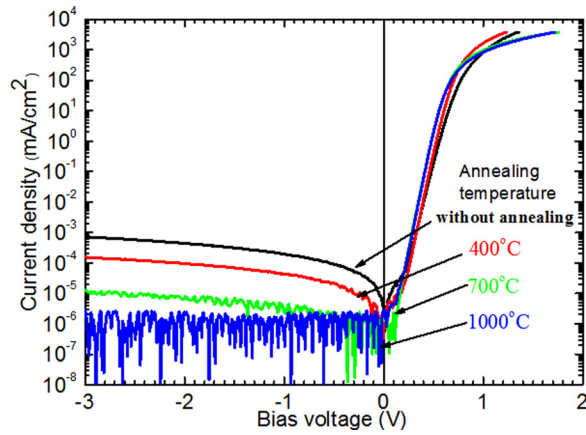


FIG. 1. I - V characteristics of p^+ -Si/ n -SiC junctions without being annealed and annealed at 400, 700, and 1000 °C measured at room temperature.

2.98×10^{-6} mA/cm². The series resistance of the junctions was extracted from the slope of the measured I - V characteristics for the forward bias voltages between 0.8 and 1.7 V. We found that the resistance increased after annealing above 700 °C, which is attributed to the oxidation of the evaporated metal for the higher annealing process. We also found that the turn-on voltage of the junctions, which was defined as the forward-bias voltage for the current of 100 mA/cm², decreased from 0.78 to 0.68 V as the annealing temperature increased. The values of parameters for the respective junctions are summarized in Table I.

The I - V characteristics of the unannealed junction and the junction annealed at 1000 °C measured at various temperatures are shown in Figs. 2(a) and 2(b), respectively. We find that the slope of the current obtained at 85, 135, and 200 °C after annealing at 1000 °C for reverse bias voltages between -1 and -3 V is not sensitive to the temperature of measurement. In comparison, the slope of the current for the unannealed junction decreases as the temperature of measurement increases.

Figures 3(a) and 3(b) show TEM images of the unannealed interface and the interface annealed at 1000 °C, respectively. An amorphous layer of ~ 6 nm thickness was formed at the interface without annealing. After annealing at 1000 °C, an abrupt interface and no amorphous layer are observed at the interface. More importantly, no structural defects such as cracks were observed at the interface whether with or without annealing.

Prior to bonding, the surfaces were irradiated by the fast atom beam of Ar in the SAB process, so that the surface states are likely to be formed at the interface.^{15–17} Such surface states should be distributed in the 6 nm thick amorphous

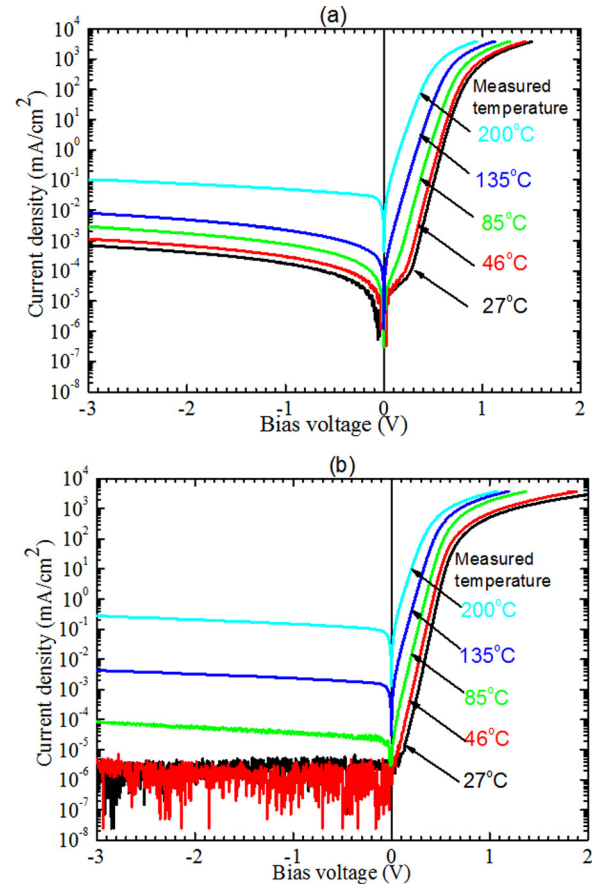


FIG. 2. I - V characteristics of p^+ -Si/ n -SiC junctions without being annealed (a) and annealed at 1000 °C (b) measured at various temperatures.

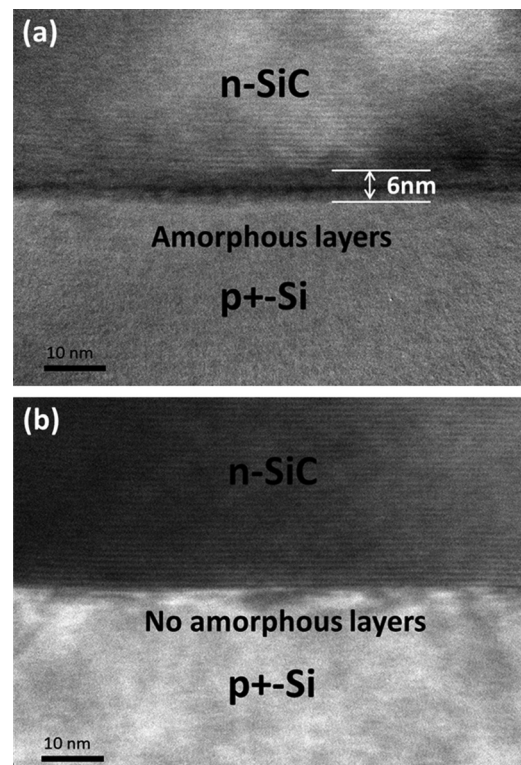


FIG. 3. TEM cross-section images of the p^+ -Si/ n -SiC interface without being annealed (a) and annealed at 1000 °C (b).

TABLE I. The reverse-bias current, turn-on voltage, ideality factor, and resistance of p^+ -Si/ n -SiC junctions.

Annealing temperature	Reverse-bias current (mA/cm ²)	Turn-on voltage (V)	Ideality factor	Resistance (Ω -cm ²)
Without annealing	7.20×10^{-4}	0.78	1.32	0.13
400 °C	1.56×10^{-4}	0.71	1.15	0.10
700 °C	1.30×10^{-5}	0.67	1.10	0.28
1000 °C	2.98×10^{-6}	0.68	1.03	0.25

layer [Fig. 3(a)]. In the I - V characteristic of p^+ -Si/n-SiC junction without annealing the magnitude of the reverse-bias current increases with increasing the bias voltage and the temperature of the measurement, similar to SAB-based p^- -Si/n $^+$ -Si junctions¹⁶ and wafer-fused p-GaAs/n-GaN heterojunctions.¹⁸ The relationship between the reverse-bias current at -3 V and the temperature of the measurement is shown in Fig. 4. The data obtained at 27 and 46 °C are not shown in this figure because they are below the resolution of the measurement unit. We found that the reverse-bias current dependence on the temperature was approximately expressed as $I \propto \exp(-E_a/kT)$, where E_a is the activation energy. The value of the activation energy was estimated to be 0.33 and 1.02 eV for the unannealed junction and junction annealed at 1000 °C, respectively.

The bias voltage and the temperature dependence of the reverse-bias current suggest that in the unannealed junctions, current generation is occurring via a two-step process at the Si/SiC interface. First, the electrons in the valence band edge of p^+ -Si were thermally excited to the interface states. Then, the electrons tunnel into the conduction band of the n-SiC. The features in the p^+ -Si/n-SiC junction after annealing at 1000 °C—such as the disappearance of the amorphous layer, and the decrease of the ideality factor to 1.03—indicated that the effects of the interface states are negligible and the diffusion current mechanism dominates the transport properties of carriers across the interface for the forward bias voltages.

The existence of amorphous layer across the unannealed interface is assumed to prohibit fracturing caused by the difference in lattice constants between Si and SiC. Neither amorphous layer nor structural defects were observed at the interface after annealing at 1000 °C, which means that the amorphous layer of the p^+ -Si/n-SiC interface was recrystallized due to such a high-temperature annealing process. Similar change in the structure of the interface was observed in the p-Si/n-GaAs and p-GaP/n-GaAs heterojunctions fabricated by SAB.^{19,20} The reduced amorphous layer thickness upon annealing is assumed to be responsible for the observed improvement of the I - V characteristics after annealing. We find that the magnitude of the reverse-bias current for higher annealing temperatures much smaller than those previously reported for n-Si/n-SiC (Ref. 21) and p-Si/n-SiC (Ref. 10)

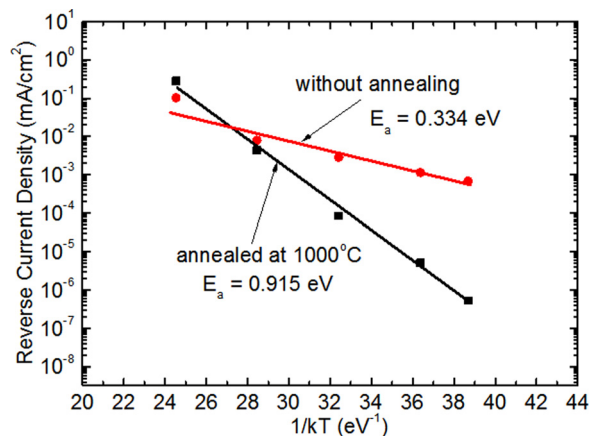


FIG. 4. Relationship of the reverse-bias current measured at -3 V for p^+ -Si/n-SiC junctions without being annealed and annealed at 1000 °C.

heterojunctions fabricated by molecular beam epitaxy or by direct wafer bonding.

Given that the high temperature (typically 1000 °C)^{22,23} process is required for forming good ohmic contacts on SiC, it is notable that the two substrates were firmly bonded to each other after annealing at 1000 °C. It is also noteworthy that (1) the reverse-bias current at -3 V decreased to 2.98×10^{-6} mA/cm² and (2) the amorphous layer vanished after annealing at 1000 °C, which suggest that the SAB-based Si/SiC junctions are anticipated to play a significant role in fabricating devices operating for high-power and high-frequency applications.

In summary, we fabricated the p^+ -Si/n-SiC junctions using the SAB and demonstrated the influence of thermal annealing process on the interface. The reverse-bias current at -3 V and the ideality factor were reduced to 2.98×10^{-6} mA/cm² and 1.03, respectively, after annealing at 1000 °C. An amorphous layer with thickness of ~ 6 nm, which was observed at the unannealed interface, disappeared after annealing at 1000 °C. Thus, the SAB technology in combination with the thermal annealing is likely to be useful for fabricating devices for high-power applications in harsh environments.

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